Orange Tree Technologies

ZestDAQ Data Acquisition and Control Platform

Simplifying data acquisition and control applications

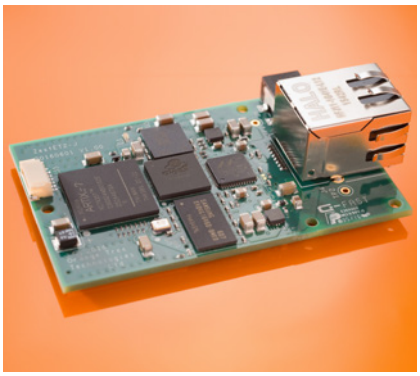
Data acquisition is an essential task in a huge variety of applications.

Just to name a few: grabbing still or video images for applications such as medical imaging, industrial inspection or security, capturing test rig data, or gathering operational data from factory automation systems. Data flow in the opposite direction in applications such as wide format or 3D printing is also increasing. The Internet of Things (IoT) is also driving new applications with sensors generating even more data.

These applications can be tricky to manage in an embedded system, with high volumes of data needing to be handled by an interface, and sent to a host PC.

Data acquisition structure

However varied the applications may be, they typically have similar requirements and a similar structure, see Figure 1. The first stage is the interface to the peripheral or sensor producing the data, which might be a camera, ADC or other sensor.



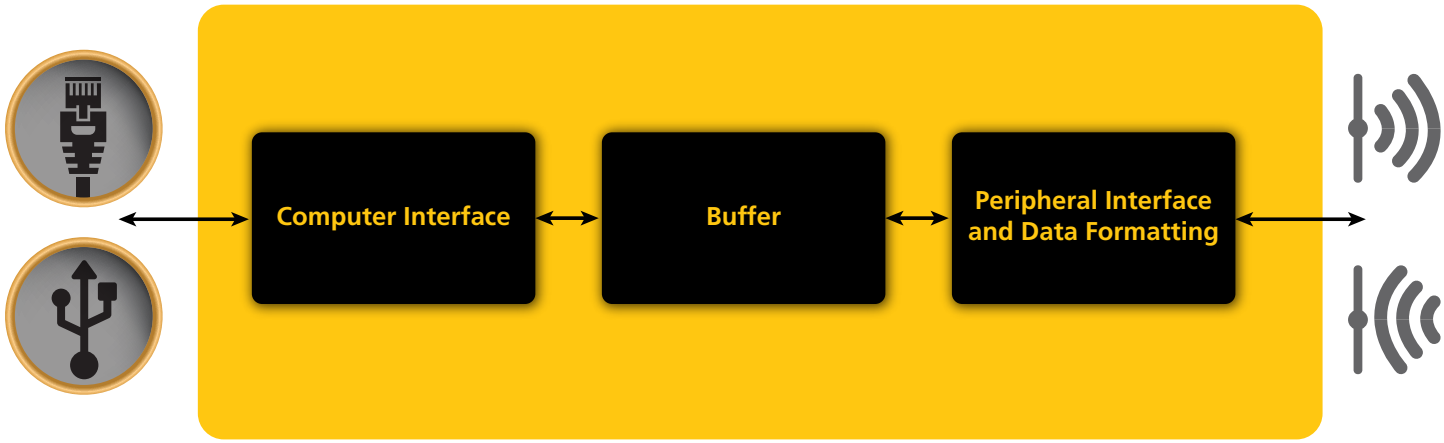


Figure 1. Typical Data Acquisition System

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The data may then be processed or formatted on the fly, and buffered in on-board memory to smooth out any bursts of data from the sensor. Finally the data is sent to a host computer for display and/or storage, often using an Ethernet or USB interface. There may also be a control channel for setting up any parameters of the acquisition system, and for starting and stopping it.

There are also, of course, applications where data flows in the other direction from a PC to transducers. For example, controlling a 3D printer requires the output of substantial amounts of data. These data output tasks require similar functions to the structure shown in Figure 1 but with the data flow reversed.

Tasks of the interface

These functions may be common, but their requirements are not trivial. Buffering the data in RAM requires handling of FIFO (first in, first out) functions, which need memory accesses to a single external RAM device to be multiplexed for simultaneous reads and writes. It may also be necessary to route multiple data streams through the FIFO, for example if images are being captured from two or more cameras.

Once the data is captured and buffered, the interface needs to send it to the host PC. This can often involve feeding multiple data channels through a single USB or Ethernet connection.

Additionally, in most applications it's necessary to process the data from the sensor before it is sent to the PC. For example, word lengths might need to be changed from 10 bit to 8 bit, or it may be required to change the format of image data, or to add frame boundaries or configure raw data to fit a higher level protocol. While it's possible to handle these changes on the PC, it is often desirable to reconfigure the data in hardware before sending it to the computer, to achieve higher speeds and to preserve host PC resources.

Standard platform

To address these challenges, Orange Tree Technologies developed its ZestDAQ software. This is a platform for data acquisition (DAQ) and control applications running on the Zest series of USB and Gigabit Ethernet boards, which provide high-speed embedded device interconnect.

Provided free of charge to Orange Tree customers, ZestDAQ consists of multiple FPGA logic cores designed to make the buffering, formatting and transfer of data between peripherals or sensors and a host PC as straightforward as possible.

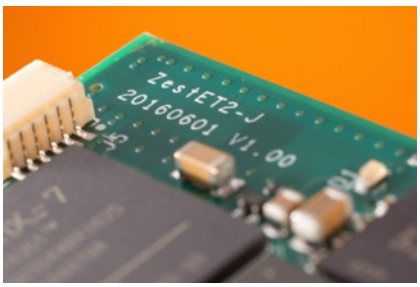
With this framework, the user needs only to create the application specific code to interface to their peripherals and format the data in a suitable manner for transmission to the host PC. This reduces the design effort for common data acquisition and control architectures, saving time for end users and enabling them to concentrate on their own specialised sensors and applications.

Common components

Block diagrams of the arrangement of the cores are shown below. Figure 2 shows the cores in a ZestET2 Ethernet board. The Ethernet wrapper bridges between the GigEx Ethernet chip on the Orange Tree board and a user friendly interface inside the FPGA, and provides simple access to 16 simultaneous channels transferring data over the network.

The wrapper includes the connection management state machine and a data multiplexor to hide the detailed operation of the GigEx device. It presents 16, byte wide parallel, bidirectional FIFOs to the user FPGA application.

Data flows through the SDRAM buffer core which makes the SDRAM device appear as multiple parallel FIFOs, allowing buffering of bulk data between the user application and the Ethernet interface. The register interface provides a simple way to read and write control and status registers inside the user application.



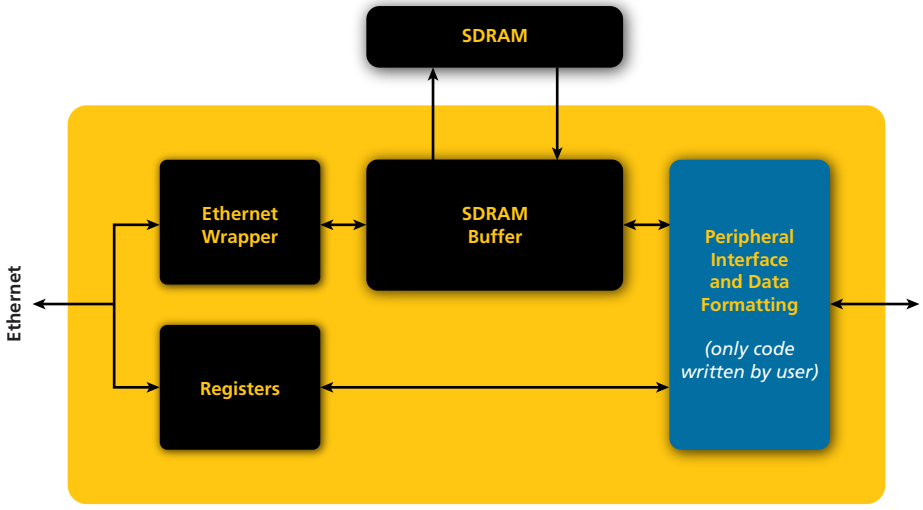


Figure 2: Arrangement of cores in a ZestET2 Ethernet board

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The diagram in Figure 3 shows the arrangement of cores in a ZestSC3 USB board. The USB interface requires the addition of the ZestSC3 USB physical core provided with that board.

The USB wrapper core provides a way of multiplexing multiple data streams over the single USB connection. A lightweight protocol is used to enable this multiplexing with minimal impact on the data transfer rate. Data is multiplexed in blocks from each channel in a round-robin fashion where more than one channel is ready to transfer data. The block length can be controlled for each channel individually, and it can be a fixed length or a variable length determined at runtime.

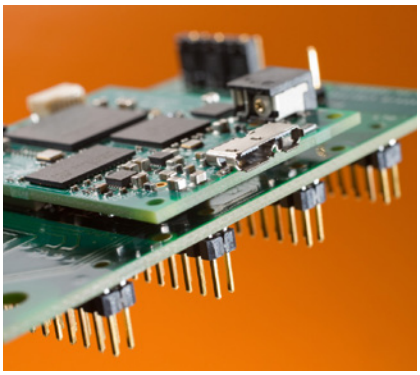
The wrapper and register cores have similar interfaces to the Ethernet versions making porting of applications between the two platforms straightforward.

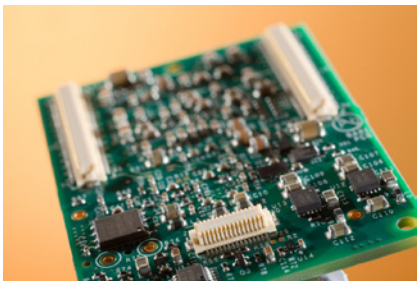
ZestDAQ provides common IP interfaces across multiple boards, which simplifies the porting of designs between Orange Tree's USB and Ethernet modules. It also includes a host software library and host software examples.

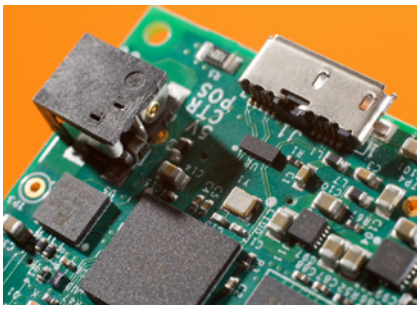
Benefits of ZestDAQ

Since many data acquisition applications have a similar structure, a standardised platform such as ZestDAQ can be invaluable. It means that customers benefit from proven, tested code, which helps to cut time to market and reduce risk.

With the ZestDAQ platform, the design effort needed for common data acquisition and control architectures is substantially reduced – saving time and reducing costs.







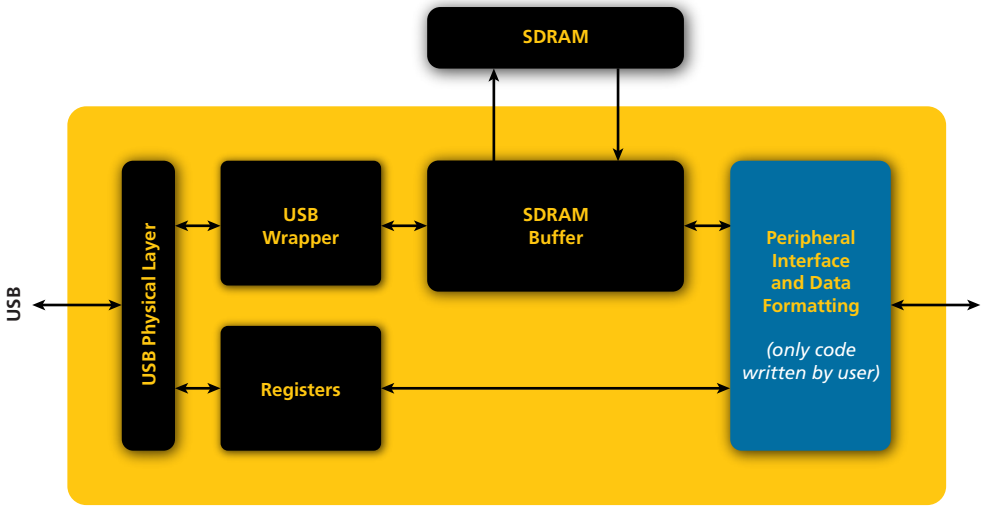


Figure 3: Arrangement of cores in a ZestSC3 USB board

The SDRAM buffer core is identical on both USB and Ethernet boards. It wraps the SDRAM memory so that it appears as up to 16 independent FIFOs. Each FIFO can have asynchronous input and output clocks and independent input and output widths of 8, 16, 32, 64 or 128 bits. Various options are provided for byte enables and packing of byte data into words as well as big and little endian support. Each channel can be assigned any address ranges in the SDRAM allowing each FIFO to be any length.

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