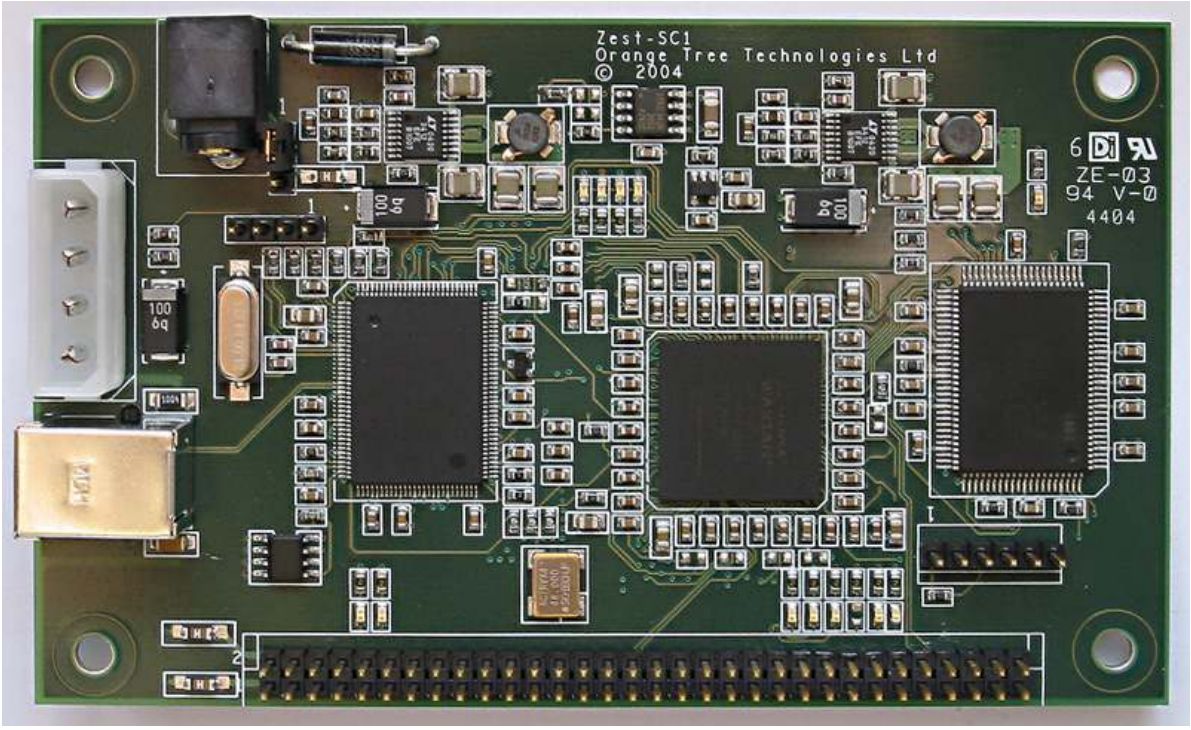
Orange Tree Technologies

ZestSC1: FPGA+USB Module

The ZestSC1 is a highly optimized FPGA module that connects to a host PC through High Speed USB 2.0 (480Mbits/s) and achieves a sustained USB bandwidth of 38MBytes/s. The board has a compact form factor (74x122mm) and is intended for applications such as semiconductor prototyping and test , DAQ, industrial control and image processing. It scales to OEM volumes and can also be used as a desk -top board for FPGA based prototyping, development, training and demonstrations.

The FPGA is a Xilinx Spartan-3 with up to 1 million gates. There are also up to 8MBytes of pipelined ZBT SRAM and 49 header pins for user I/O. The board can be powered entirely from the USB port, or if more than 2.5W is required it can be powered from a wall adapter or hard disk drive power connector. The board features standard 0.1" pitch connectors for maximum flexibility.

Provided with the ZestSC1 are libraries and IP to support an easy to use, out-of-the-box experience. This includes: host support software including a system driver and a host library; USB interface; SRAM interface; HDL testbenches; multiple design examples that consists of a host program and a VHDL and Verilog project (including source). All the board needs to operate is a USB cable connected to a PC.



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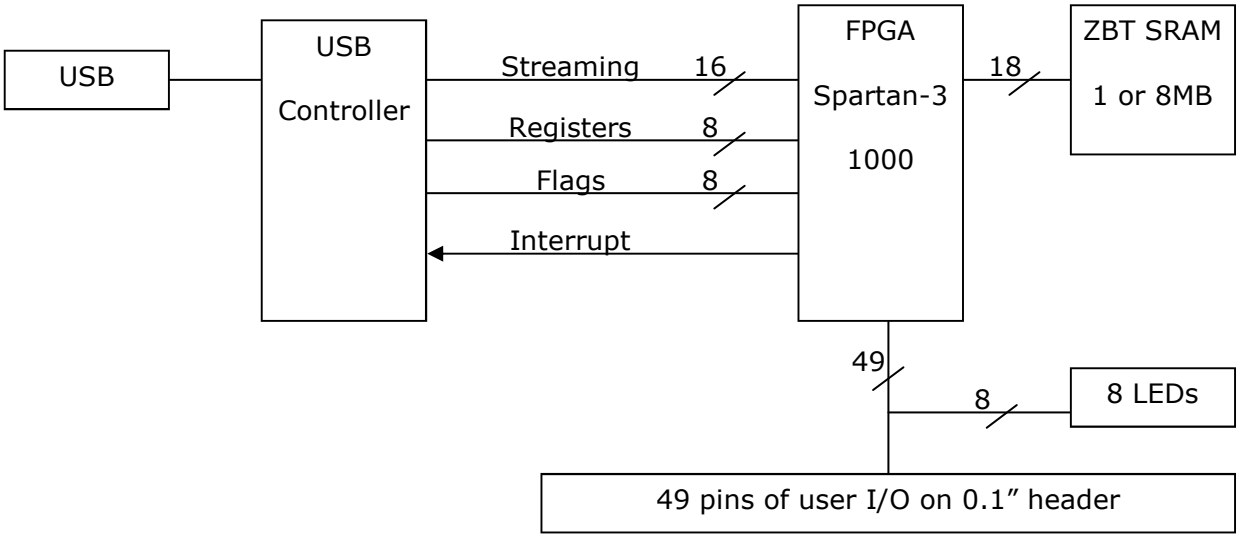

USB	High Speed USB 2.0 (480Mbits/s burst, up to 38MBytes/s sustained (dependent on host)) or Full Speed USB 1.1 (12Mbits/s burst). Cypress EZ-USB FX2 USB microcontroller chip.
FPGA	Xilinx Spartan-3 XC3S1000-4 in FT256 package Configured from USB, or Xilinx Parallel Cable IV with JTAG
Host communications	Three interfaces between FX2 and FPGA all accessible using host library supplied with board: Streaming—data streaming at the maximum USB bandwidth; Registers—control and status registers in FPGA application; Signalling—single bit interrupt and flags.
Memory	Pipelined ZBT SRAM 512K x 18 or 4M x 18 ZBT is "Zero Bus Turnaround" for no wait states between writes and reads
I/O	64-pin 0.1" header for ribbon cable or daughter card (for example ADC/DAC, video) 49 pins connected to FPGA for user I/O 12 pins connected to ground, 1 pin connected to 5V, 1 pin connected to 3.3V, 1 pin connected to ground (default) or FPGA I/O voltage FPGA I/O voltage either 3.3V (default) or from IO pin
LED's	8 LED's connected to 8 I/O pins, active low 4 LED's for power indication/ 1 LED for FPGA Done signal
FPGA Clocks	Fixed 48MHz for streaming interface between FX2 and FPGA Fixed 48MHz for microcontroller registers interface between FX2 and FPGA I/O input clock from I/O header—single ended or differential FPGA can synthesise internal clocks from 1.5MHz to 280MHz from the above clock inputs
Power	Up to 95% efficient on-board PSU enables the board to be either bus-powered from a high power USB port; or self-powered from a wall adapter or hard disk power connector (both nominal 5V) for higher power applications or when a low power USB port is used.
Software	Host library and drivers for configuring FPGA and communicating with the FPGA, which run on Windows / Linux, for other operating systems please enquire Free Xilinx design tool ISE WebPACK available from http://www.xilinx.com/ise/logic_design_prod/webpack.htm
Logic cores	FPGA interfaces for FX2 and SRAM—cores and testbenches in both VHDL and Verilog
Examples	C, VHDL and Verilog source code for various examples
Physical	74 x 122 mm

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